



## RESPONSE UNDER 37 C.F.R. § 1.116 EXPEDITED PROCEDURE REQUESTED EXAMINING GROUP 2123

PATENT Customer No. 22,852 Attorney Docket No. 04173.0441

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)
Hisashi Kaneko et al.	) Group Art Unit: 2123
Application No.: 10/757,415	) Examiner: Sharon, Ayal
Filed: January 15, 2004	) Confirmation No. 3384
For: SIMULATION CIRCUIT PATTERN EVALUATION METHOD, MANUFACTURING METHOD OF SEMICONDUCTOR INTEGRATE CIRCUIT, TEST SUBSTRATE, AND TEST SUBSTRATE GROUP	) Mail Stop AF ) ) )

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

## **AMENDMENT AFTER FINAL**

In reply to the Final Office Action mailed May 22, 2007, the period for response being on August 22, 2007, and pursuant to 37 C.F.R. § 1.116, Applicants propose that this application be amended as follows:

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks begin on page 7 of this paper.